REMARKS

The Office Action mailed on February 7, 2005 has been received and its contents carefully considered. In this submission, Applicants have amended claim 13 to correct an inadvertent informality. Claims 12 and 15 are cancelled. Claims 9 and 13 are the independent claims. Claims 9-11 and 13-14 remain pending in the application. For at least the following reasons, it is submitted that all pending claims are in condition for allowance.

The title of the invention is amended herein to be clearly indicative of the invention to which the claims are directed.

Claims 12 and 15 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. In particular, the Office Action alleged that the pending claims state that "the source/drain electrodes comprise an ohmic contact layer (in claims 12 and 15) and the stacked structures comprises an ohmic contact layer (in claims 9 and 13) which is different from the ohmic contact layer of the source/drain electrodes," while the Description states that "there is only one ohmic contact layer (Paragraph [0010])". In response, claims 12 and 15 have been cancelled. The rejection is therefore moot.

Claims 9 to 12 have been tentatively rejected under 35 U.S.C. 103(a) as allegedly obvious over *Tsujimura et al.* (U.S. Patent Application No. 2002/0190253), *Licari et al.* (U.S. Patent No. 5,485,038) and *Gee-Sung et al.* (U.S. Patent No. 5,998,230) Claim 12 has been cancelled . For at least the reasons set forth below, Applicant submits that these rejections should be withdrawn.

Applicant's independent claim 9 recites a thin film transistor (TFT) structure, which includes a plurality of stacked structures, a photo-imagable layer, a source electrode and a drain electrode, a passivation layer, and a transparent electrode. The stacked structures are disposed on

a substrate and include a first conducting layer, an insulation layer, and an amorphous silicon layer. The photo-imagable layer is disposed between the stacked structures. **The source electrode and drain electrode** are disposed **on the photo-imagable layer**. The source electrode is connected to a portion of the amorphous silicon layer and the drain electrode is connected to another portion of the amorphous silicon layer. **The passivation layer** is disposed **on the amorphous silicon layer**, the source electrode and the drain electrode. The transparent electrode is disposed on the passivation layer and electrically connected to one of the source electrode and the drain electrode.

In contrast, *Tsujimura et al.* appear to disclose a thin film transistor including a substrate 20, a gate electrode 21, a gate insulating layer 22, a semiconductor layer 23, a channel protection layer 24, source and drain electrodes 25, 26, a passivation layer 27, a interlayer insulator 31, and a pixel electrode 32. The gate insulating layer 22 is deposited on the substrate 20 and the gate electrode 21 formed thereon. The semiconductor layer 23 is deposited on the gate insulating layer 22. The channel protection layer 24 is deposited on the semiconductor layer 23 in order to protect the semiconductor layer 23 from ion injection. (paragraph [0051]; and FIG. 3) The interlayer insulator 31 is formed on the passivation layer 27, and the passivation layer 27 is deposited to cover the underlying substrate 20, channel protection layer 24, and source and drain electrodes 25, 26, except for contact holes 28 at the drain electrode 26. The pixel electrode 32 is formed on the interlayer insulator 31 and the drain electrode 26 via openings of the interlayer insulator 31.

The Office Action indicates that *Tsujimura et al.* do not show the first stacks including an ohmic contact layer and the interlayer made of photo-imagable material, but relies on *Gee-Sung*

et al. to teach an ohmic layer in a stacked structure and *Licari et al.* to use photo-imagable material for interlayers.

However, there is no disclosure or a suggestion by *Tsujimura et al.* that the passivation layer is disposed on the amorphous silicon layer, as recited in claim 9. The channel protection layer 24 of *Tsujimura et al.* is deposited on the semiconductor layer 23 instead, and the passivation layer 27 is then deposited to cover the channel protection layer 24.

Further, *Tsujimura et al.* fail to disclose or suggest that the source electrode and drain electrode are disposed on the photo-imagable layer, as recited in claim 9. Rather, the interlaying insulator 31 of *Tsujimura et al.* relied upon by the Examiner as being the photo-imagable layer is disposed above the source and drain electrodes 25, 26. As is clear from FIG. 3, the spatial relationship of the source/ drain electrode and the alleged photo-imagable layer in *Tsujimura et al.* is upside down from the present invention.

Moreover, neither *Gee-Sung et al* nor *Licari et al.* overcome the deficiencies of *Tsujimura et al.* As such, the claimed structure is not disclosed nor suggested by *Tsujimura et al* alone nor in combination with *Gee-Sung et al,* and *Licari et al.* It is therefore submitted that the claim 9 is patentable over the cited references. Claims 10-11 are also patentable over the cited references for at least the reasons advanced above as to the patentability of independent claim 9, from which these claims respectively depend, as well as for the additional features they recite. Therefore, claims 9-11 are not rendered obvious by the cited reference and the rejection should be withdrawn.

Claims 13 to 15 have been rejected under 35 U.S.C. 103(a) as allegedly unpatentable over *Tsujimura et al.*, *Licari et al.* and *Gee-Sung et al.*, as applied to claim 13 above, and further in

view of *Ota et al.* (JP 06-084946). Claim 15 has been cancelled. It is submitted that claims 13-14 are patentable over the cited references.

Applicant's independent claim 13 recites a thin film transistor (TFT) structure, which includes a plurality of first stacked structures and second stacked structures, a photo-imagable layer, a source electrode and a drain electrode, a passivation layer, and a transparent electrode. The first stacked structures are disposed on a substrate and include a first conducting layer, an insulation layer, and an amorphous silicon layer. The second stacked structures are disposed on a substrate and include the first conducting layer. The photo-imagable layer is disposed between the stacked structures. The source electrode and drain electrode are disposed on the photo-imagable layer and the first stacked structures. The source electrode is connected to a portion of the amorphous silicon layer and the drain electrode is connected to another portion of the amorphous silicon layer. **The passivation layer** is disposed **on the amorphous silicon layer,** the photo-imagable layer and the source electrode and the drain electrode. The transparent electrode is disposed on the passivation layer; a first portion of the transparent electrode electrically connects to one of the source electrode and the drain electrode; and a second portion of the transparent electrode electrically connects to the second conducting layer of the first stacked structures and the first conducting layer of the second stacked structure.

The Office Action indicates that *Tsujimura et a., Licari et al. and Gee-Sung et al.* do not show the source/drain electrodes and said passivation layer on said photo-imagable interlayer, but relies on *Ota et al.* to teach the source/drain electrodes and said passivation layer on said photo-imagable interlayer to improve alignment.

However, there is no disclosure or a suggestion by *Tsujimura et al.* that the passivation layer is disposed on the amorphous silicon layer, as recited in claim 13. Rather, the channel

protection layer 24 of *Tsujimura et al.* is deposited on the semiconductor layer 23, and the passivation layer 27 is then deposited to cover the channel protection layer 24. Moreover, neither *Gee-Sung et al,* nor *Licari et al., nor Ota et. al.* overcome the deficiencies of *Tsujimura et al.* As such, the claimed structure is not disclosed nor suggested by *Tsujimura et al* alone nor in combination with *Gee-Sung et al, Licari et al., and/or Ota et. al.* For at least this reason, claim 13 is patentable over the cited references. Claim 14 is also patentable over the cited references for at least the reasons advanced above as to the patentability of independent claim 13, from which these claims respectively depend, as well as for the additional features they recite. Therefore, claims 13-14 are not rendered obvious by the cited reference and the rejection should be withdrawn.

Based on the above, it is submitted that all pending claims of this application are in condition for allowance and such a Notice, with allowed claims 9-11 and 13-14, earnestly is solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: _____
Daniel R. McClure
Registration No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500